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ARRANGEMENT FOR TESTING NETWORK SWITCH EXPANSION PORT DATA BY CONVERTING TO MEDIA INDEPENDENT INTERFACE FORMAT

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the testing of network devices such as integrated network switches configured for switching data packets between subnetworks.

BACKGROUND ART

Local area networks use a network cable or other media to link stations on the network. Each local area network architecture uses a media access control (MAC) enabling network interface devices at each network node to access the network medium.

Switched local area networks such as Ethernet (IEEE 802.3) based systems are encountering increasing demands for higher speed connectivity, more flexible switching performance, and the ability to accommodate more complex network architectures. For example, commonly-assigned U.S. Patent No. 5,953,335 discloses a network switch configured for switching layer 2 type Ethernet (IEEE 802.3) data packets between different network nodes. Hence, network switch designers and test engineers need to be able to minimize the time and expense needed to evaluate designs during prototyping of Ethernet-based network systems.

One problem associated with testing network-based switch chips involves the limited availability of the sample chips for testing hardware associated with interaction between multiple chips. For example, the network switch disclosed in U.S. Patent No. 5,953,335 describes an expansion port that may be used for interconnecting multiple network switch chips for transfer of packet data according to a prescribed bus protocol, such as peripheral component interconnect (PCI) bus protocol. However, use of the expansion port assumes the availability of at least one additional network switch chip for interconnection of the expansion ports of the respective network switch chips.

Hence, there is a concern that the expansion port and associated operations cannot be tested or validated if only one network switch chip is available for testing. In addition, even if a second network switch chip was available for testing of the expansion ports, a detected error between the expansion port operations creates the additional problem of determining whether the detected error is due to a problem in the first switch chip under test, a problem in the second switch chip used for testing the

expansion port of first switch chip, a problem in the connection between the two expansion ports, or any combination of the foregoing.

SUMMARY OF THE INVENTION

There is a need for an arrangement that enables an expansion port of a network switch chip, configured for transferring data according to a prescribed bus protocol, to be tested and evaluated without the necessity of a second switch chip.

This and other needs are attained by the present invention, where a network switch chip having an expansion port configured for transferring data according to a prescribed bus protocol is tested using test equipment and a converter. The test equipment includes a media independent interface (MII) configured for sending and receiving data according to a prescribed network protocol, and a converter is configured for converting data between the prescribed bus protocol and the prescribed network protocol. Hence, the expansion port of the network switch chip can be tested without the necessity of a second network switch chip.

One aspect of the present invention provides a method for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol. The method includes outputting the data from the expansion port according to the prescribed protocol, converting the data from the prescribed protocol to a prescribed network protocol, and outputting the data according to the prescribed network protocol to a test device having an interface configured for receiving the data according to the prescribed network protocol. The conversion of the data from the prescribed protocol to the prescribed network protocol enables the use of the test device for validation of the expansion port, without the necessity of another network switch chip.

Another aspect of the present invention provides a test system configured for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol. The test system includes a test device configured for outputting and receiving data according to a media independent interface (MII) protocol, and a converter. The converter is configured for converting the data between the MII protocol utilized by the test device and the prescribed protocol utilized by the expansion port, enabling communication between the expansion port and the test device. Hence, the expansion port of the network switch chip can be tested without the necessity of a second switch chip having a corresponding expansion port.

Additional advantages and novel features of the invention will be set forth in part in the description which follows and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The advantages of the present

invention may be realized and attained by means of instrumentalities and combinations particularly pointed in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference numeral designations represent like elements throughout and wherein:

Figure 1 is a block diagram of a system configured for testing an expansion port of a network switch chip according to an embodiment of the present invention.

Figures 2A and 2B are diagrams illustrating IEEE 802.3-based media independent interface (MII) protocol data frames and an expansion port protocol frame, respectively.

Figures 3A and 3B are diagrams summarizing testing methods including converting and outputting data from an expansion port format to an MII format, and from an MII format to an expansion port format, respectively, according to an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 is a block diagram illustrating a testing system 10 configured for testing a network switch chip 12, for example an integrated network switch as illustrated in U.S. Patent No. 5,953,335, according to an embodiment of the present invention. In particular, the network switch chip 12 includes network switch ports 14 configured for sending and receiving data frames 50, illustrated in Figure 2A, according to a prescribed network protocol, such as IEEE 802.3-based Media Independent Interface (MII) protocol. The network switch 14 also includes an expansion port 16 configured for transferring data 52, also referred to as expansion port frames, between other switch chips via their respective switch ports according to a prescribed protocol, for example a burst-based bus protocol.

The testing system 10 also includes a test device 18 configured for outputting and receiving data frames 50 according to the IEEE 802.3-based MII protocol. In particular, the test device 18 is configured for sending and receiving data packets 50 across an MII cable 20 to Ethernet-based (IEEE 802.3) devices under test in accordance with prescribed test operations via a MII connection 22. As described above, the MII connection 22 could be directly connected to any one of the network switch ports 14, however the expansion port 16 cannot be tested solely using the MII connection 22 and MII cable 20.

According to the disclosed embodiment, the test system 10 includes a converter 30 configured for converting the data between the MII protocol (e.g., data frames 50), utilized by the MII connection

22 of the test device 18, and the burst-based bus protocol (e.g., expansion port frames 52) utilized by the expansion port 16. Hence, the converter 30 enables communication between the expansion port 16 and the test device 18.

The converter 30, implemented for example using a PC board, includes first-in first-out (FIFO) buffers 32a and 32b, and a field programmable gate array (FPGA) 34. The FIFO buffers 32 are configured for storing at least one maximum-sized frame; in particular, the FIFO 32a is configured for storing at least the maximum size of the expansion port frame 52 (e.g., 1526 bytes) illustrated in Figure 2B, and the FIFO 32b is configured for storing at least the maximum sized IEEE 802.3 frame; since the FIFO 32b can receive either an untagged frame 50a or a tagged frame 50b, the FIFO 32b is configured for receiving at least the maximum size of the larger tagged frame 50b (e.g., 1522 bytes). The field programmable gate array 34 is configured for converting between the expansion port frame data and the IEEE 802.3 frame, described below.

Figure 3A is a diagram illustrating the method of testing the network switch chip according to an embodiment of the present invention. The method begins in step 60, where the converter 30 receives the expansion port frame as burst traffic and stores in step 62 the burst traffic (as an expansion port frame) in the FIFO 32a. In particular, data is transferred over the expansion bus 36 on the expansion port transmit data path (ETXD1) in bursts of eight clock (ETX_CLK = ERX_CLK) cycles; the data includes start and end of frame information as well as frame data. As described above, the expansion port data also includes the device ID field 54 illustrated in Figure 2B.

The FPGA 34 asserts the expansion port receiver request signal (ERX_REQ2) until detecting that the FIFO 32a is full. Hence, the expansion port 16 continues to transmit data so long as the expansion port receiver request (ETX_REQ2) signal (i.e., the expansion port transmit grant (ETX_GNT1) input) is asserted by the FPGA 34; in other words, the expansion port 16 continues to transmit data as long as the expansion port transmit grant (ETX_GNT1) input is asserted. Control information such as start and stop markers that correspond to data, is supplied by the expansion port 16 on the expansion port control data lines (ETX_INFO1, ERX_INFO2). The expansion port transmit start of burst (ETX_SB1) is used by the expansion port 16 to indicate to the FPGA 34 on the expansion port receive start of burst (ERX_SB2) input that valid data will be presented on the expansion port transmit data (ETXD1) path for a burst of eight clock cycles.

Once a full expansion port frame 52 has been stored in the expansion port FIFO 32a, the FPGA 34 converts in step 64 the expansion port frame 52 into an IEEE 802.3-based MII format frame 50 by removing the device identifier field 54. The FPGA 34 then outputs in step 66 the converted MII-format frame onto the MII cable 20 as a serial data stream. As illustrated in Figure 1, the FPGA 34 acts as a physical layer transceiver for the MII Interface 22 by outputting the data on a receive data

path (RXD) based on a receive clock (RX_CLK) signal, and by asserting carrier sense (CRS) and data valid (RX_DV) signals. If an error is detected by the FPGA 34 in the received expansion port frame 52, the FPGA 34 may output an error signal (RX_ER) on the MII cable 20.

Figure 3B is a diagram illustrating the method of testing the expansion port 16 by converting an IEEE 802.3 frame 50, received from the MII interface 22, into an expansion port frame 52 for transfer to the expansion port 16 according to an embodiment of the present invention. The MII FIFO 32b stores in step 70 the IEEE 802.3 frame 50, received on the transmit data (TXD) path based on the transmit clock (TX_CLK) signal and the transmit enable (TX_EN) signal. Transmit errors are indicated by the test equipment MII interface 22 outputting the transmit error (TX_ER) signal onto the MII cable 20.

The FPGA 34 converts in step 72 the stored IEEE 802.3 frame 50 into an expansion port frame 52 by inserting a device identifier field 54 having a prescribed value. The FPGA 34 then outputs in step 74 the converted expansion port frame onto the expansion port bus 36 for reception by the expansion port 16. In particular, the FPGA 34 waits until the expansion port receiver request signal (ETX_REQ1) is asserted by the expansion port 16. The FPGA 34 continues to transmit data so long as the expansion port receiver request (ETX_REQ1) signal (i.e., the expansion port transmit grant (ETX_GNT2) input) is asserted by the expansion port 16. Control information such as start and stop markers that correspond to data, is supplied by the FPGA 34 on the expansion port control data lines (ETX_INFO2, ERX_INFO1). The expansion port transmit start of burst (ETX_SB2) is used by the FPGA 34 to indicate to the expansion port 16 on the expansion port receive start of burst (ERX_SB1) input that valid data will be presented on the expansion port transmit data (ETXD2) path for a burst of eight clock cycles (ETX_CLK and ERX_CLK).

According to the disclosed embodiment, an expansion port of a network switch chip is tested using a test device having an MII interface by converting the data from the expansion port format to the MII interface format, and outputting the converted data according to the corresponding transmission format. Hence, the expansion port can be tested without the necessity of a second network switch chip; in addition, testing of the expansion port using the disclosed arrangement improves testing integrity by eliminating the possibility of failures in a second network switch chip adversely affecting testing of the expansion port of the device under test.

Although the disclosed arrangement describes conversion to a media independent interface, the expansion port data also may be converted to a reduced media independent interface (RMII) format according to the RMII™ Specification, Revision 1.2.

While this invention has been described with what is presently considered to be the most practical preferred embodiment, it is to be understood that the invention is not limited to the disclosed

embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.